Bhavnagarwala et al.

YOR920030289US1 (TAD) (8728-635)

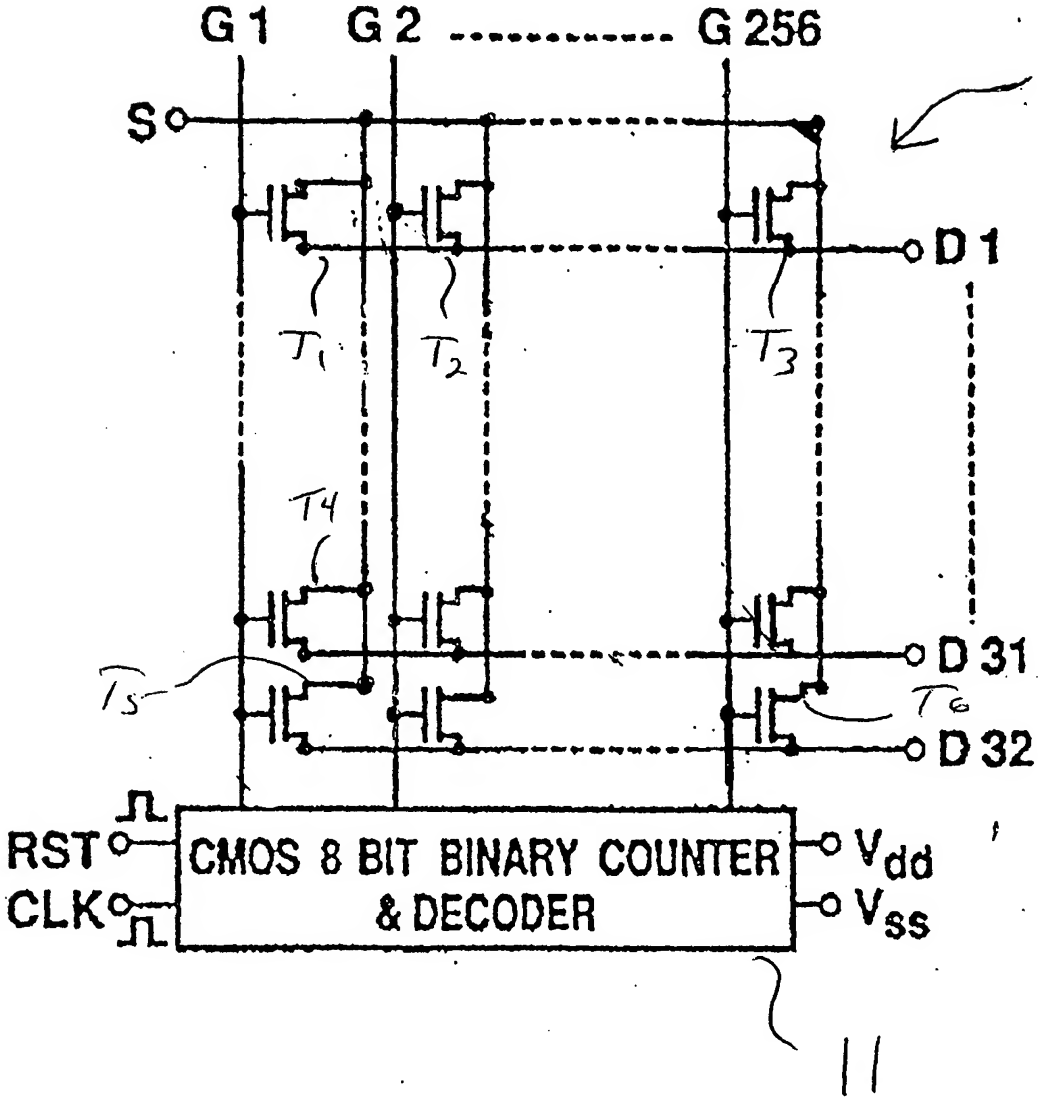


Fig. 1

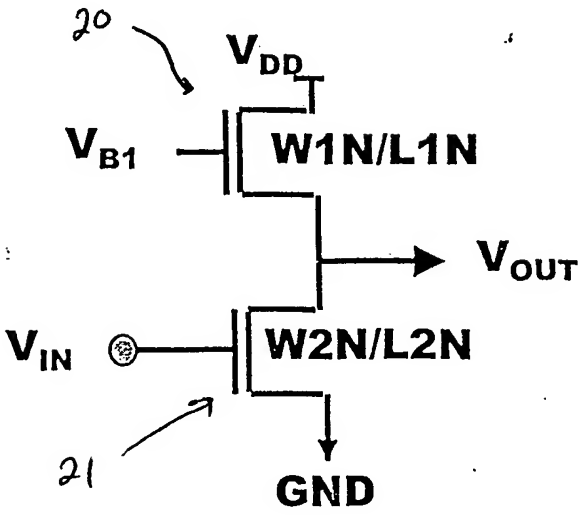


Fig 2

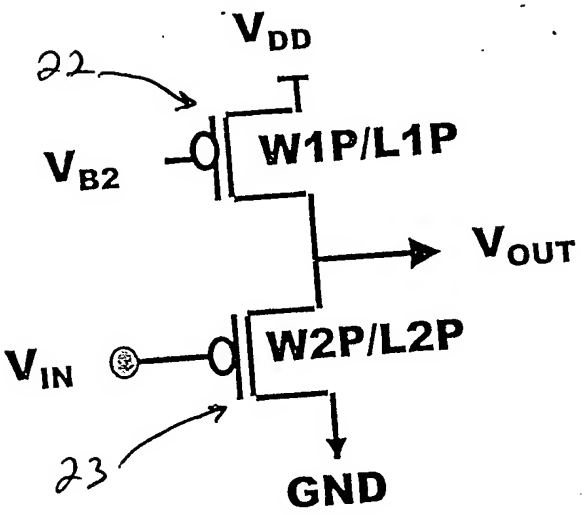


Fig 3

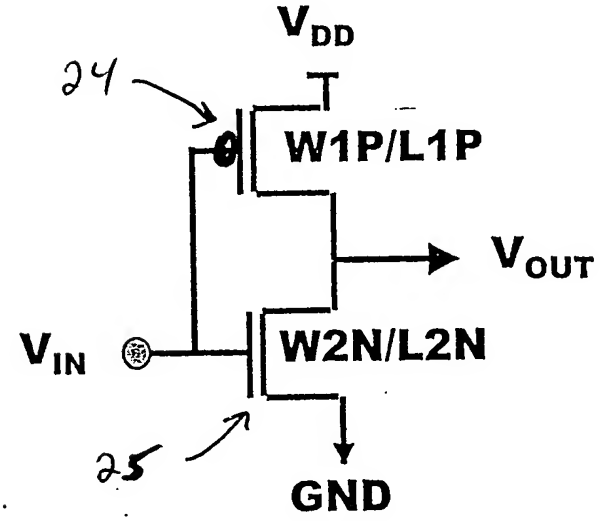


Fig 4

$$V_{in} = V_{dd} - V_{out} + \boxed{(V_{TN2} - V_{TN1})} + \boxed{\frac{\eta}{\beta} \ln \left| \frac{k_{N1}}{k_{N2}} \right|} + \frac{\eta}{\beta} \ln \left| \frac{1 - e^{-\beta(V_{dd} - V_{out})}}{1 - e^{-\beta(V_{out})}} \right|$$

$$k_{N1} = \frac{W_{N1}}{L_{N1}} \mu_{on} C_{ox} \frac{\eta}{\beta^2} \quad k_{N2} = \frac{W_{N2}}{L_{N2}} \mu_{on} C_{ox} \frac{\eta}{\beta^2}$$

(a)

(b)

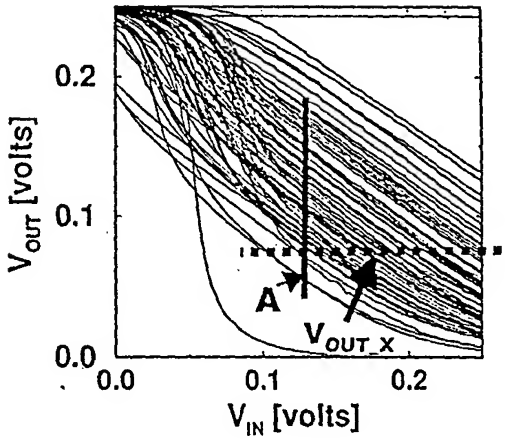


Fig. 5

II

$$V_{in} = V_{out} - \boxed{(V_{TP2} - V_{TP1})} - \boxed{\frac{\eta}{\beta}\ln\left|\frac{k_{P1}}{k_{P2}}\right|} - \frac{\eta}{\beta}\ln\left|\frac{1 - e^{-\beta(V_{dd}-V_{out})}}{1 - e^{-\beta(V_{out})}}\right|$$

$$k_{P1} = \frac{W_{P1}}{L_{P1}}\mu_{op}C_{ox}\frac{\eta}{\beta^2} \quad k_{P2} = \frac{W_{P2}}{L_{P2}}\mu_{op}C_{ox}\frac{\eta}{\beta^2}$$

Fig. 6

III

$$V_{in} = \frac{V_{dd}}{2} - \boxed{\frac{V_{tN1} - |V_{tP1}|}{2}} + \boxed{\frac{\eta}{2\beta}\ln\left|\frac{k_{P1}}{k_{N1}}\right|} + \frac{\eta}{2\beta}\ln\left|\frac{1 - e^{-\beta(V_{dd}-V_{out})}}{1 - e^{-\beta V_{out}}}\right|$$

$$k_{P1} = \frac{W_{P1}}{L_{P1}}\mu_{op}C_{ox}\frac{\eta}{\beta^2} \quad k_{N1} = \frac{W_{N1}}{L_{N1}}\mu_{on}C_{ox}\frac{\eta}{\beta^2}$$

Fig 7(a)

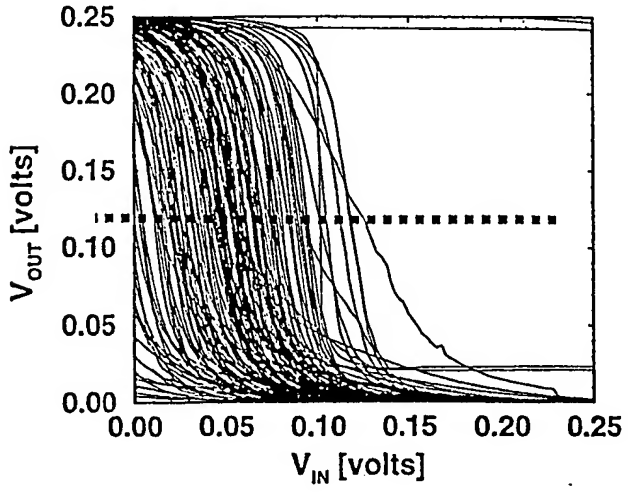


Fig. 7(b)

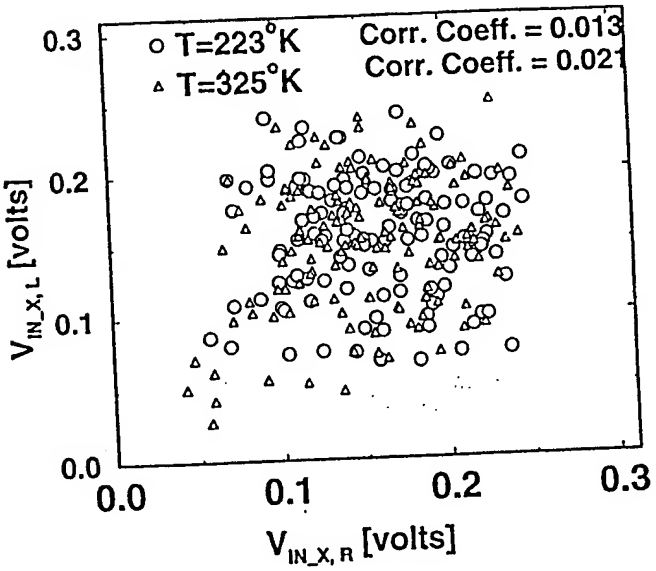

T=223°K
T=325°K
Corr. Coeff. = 0.013
Corr. Coeff. = 0.021
0.3
0.2
0.1
0.0
0.0
0.1
0.2
0.3
$V_{IN_X,L}$ [volts]
$V_{IN_X,R}$ [volts]

Fig. 8

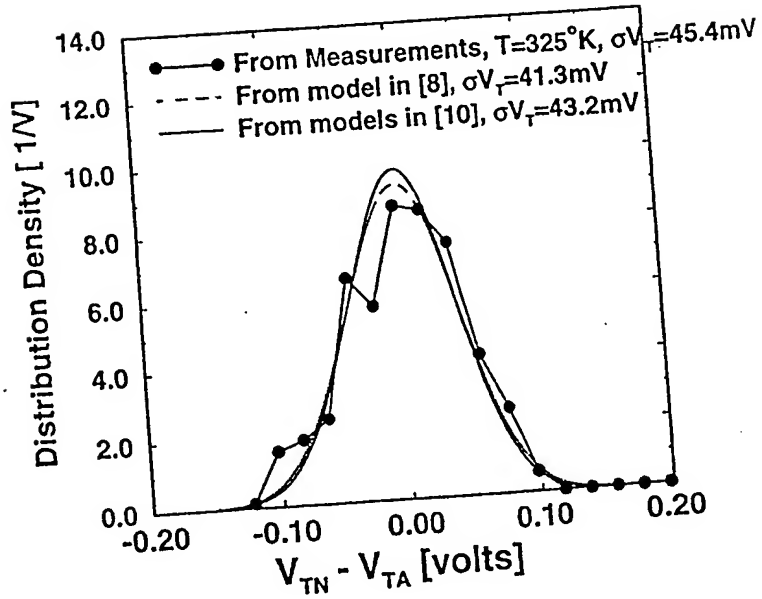

From Measurements, T=325°K, σV_T=45.4mV
From model in [8], σV_T=41.3mV
From models in [10], σV_T=43.2mV
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
-0.20
-0.10
0.00
0.10
0.20
Distribution Density [1/V]
V_{TN} - V_{TA} [volts]

Fig. 9

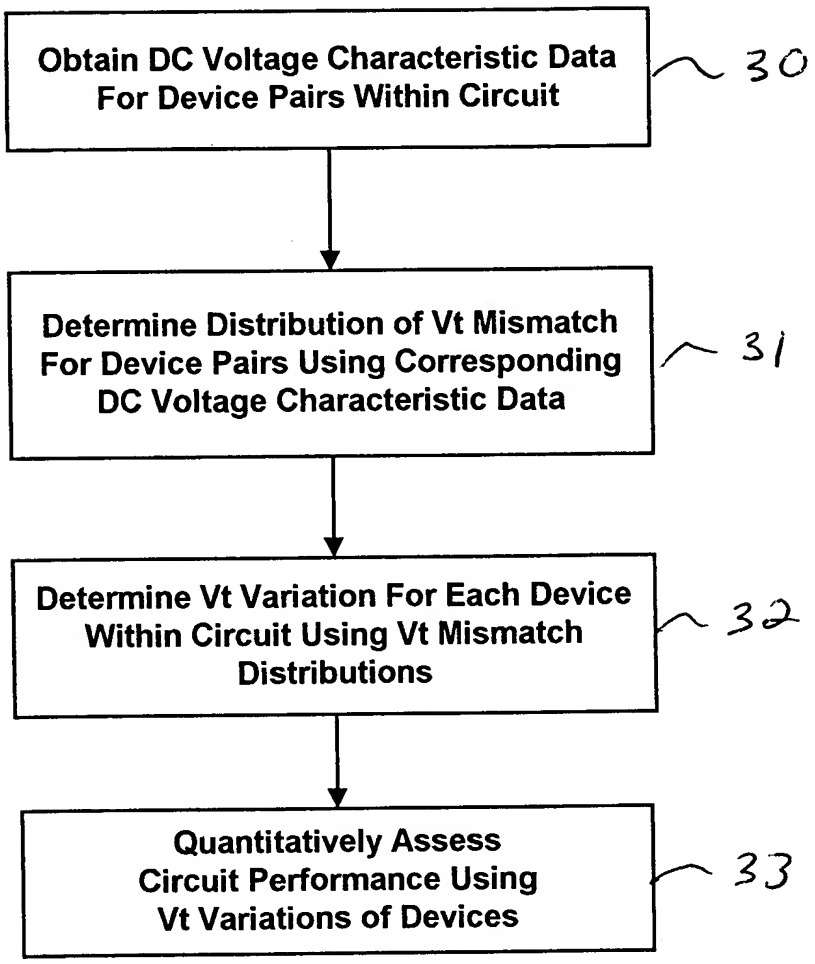

Obtain DC Voltage Characteristic Data For Device Pairs Within Circuit
30
Determine Distribution of Vt Mismatch For Device Pairs Using Corresponding DC Voltage Characteristic Data
31
Determine Vt Variation For Each Device Within Circuit Using Vt Mismatch Distributions
32
Quantitatively Assess Circuit Performance Using Vt Variations of Devices
33

Fig. 10

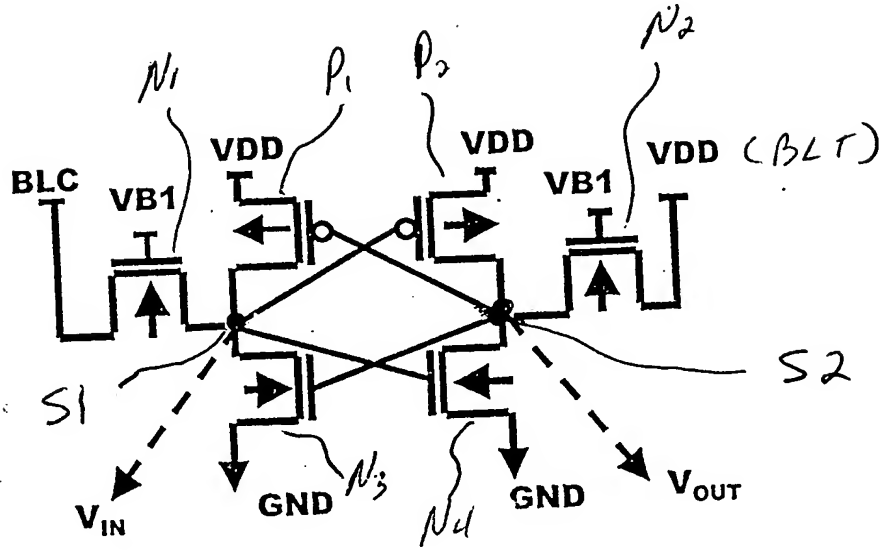

N1
P1
P2
N2
VDD
VDD
VDD (BLT)
BLC
VB1
VB1
S1
S2
VIN
GND
N3
N4
GND
VOUT

Fig. 11

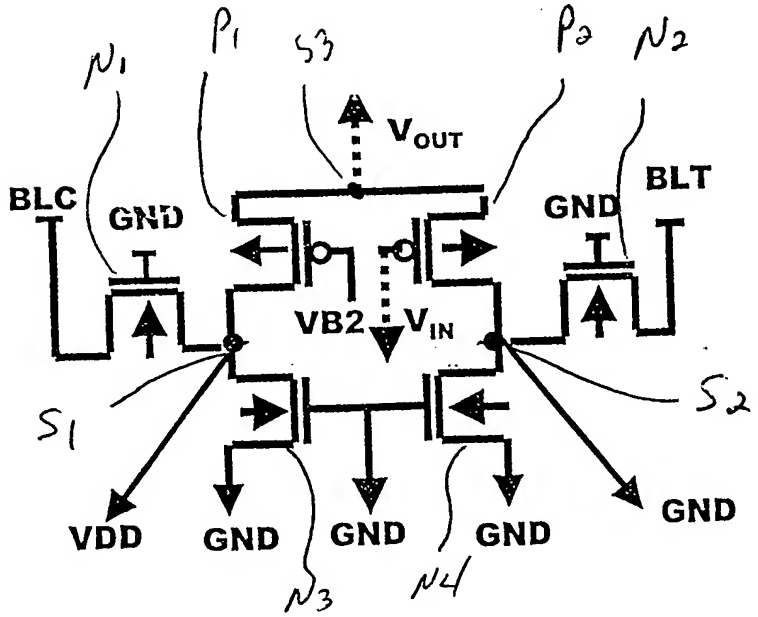

N1
P1
S3
P2
N2
VOUT
BLC
GND
GND
BLT
VB2
VIN
S1
S2
VDD
GND
GND
GND
GND
N3
N4

Fig. 12

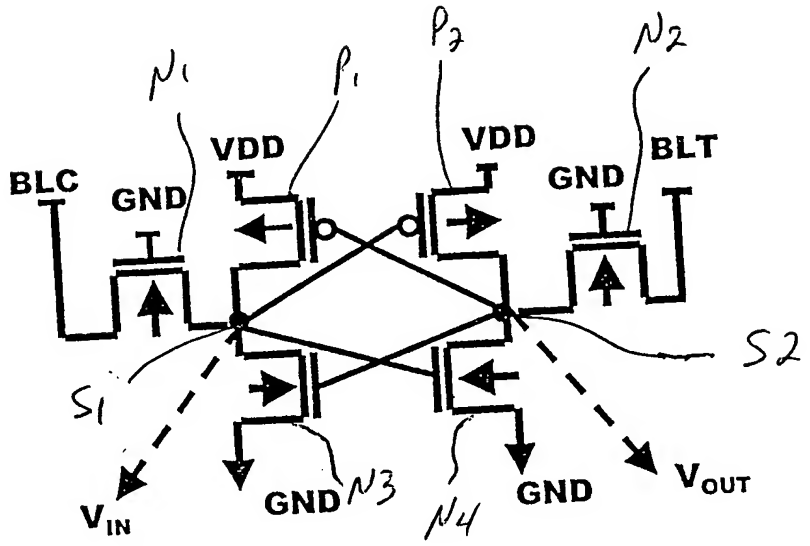

N1
P1
P2
N2
VDD
VDD
BLC
GND
GND
BLT
S1
S2
VIN
GND
N3
N4
GND
VOUT

Fig. 13

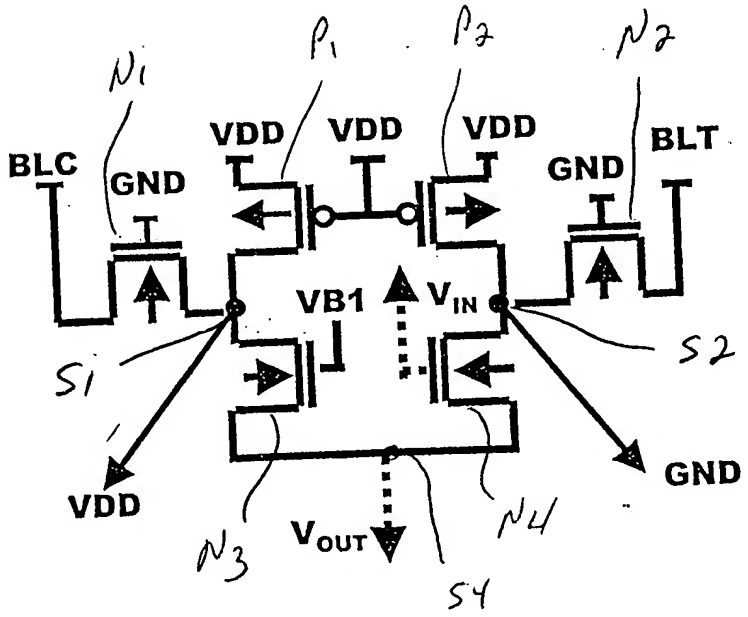
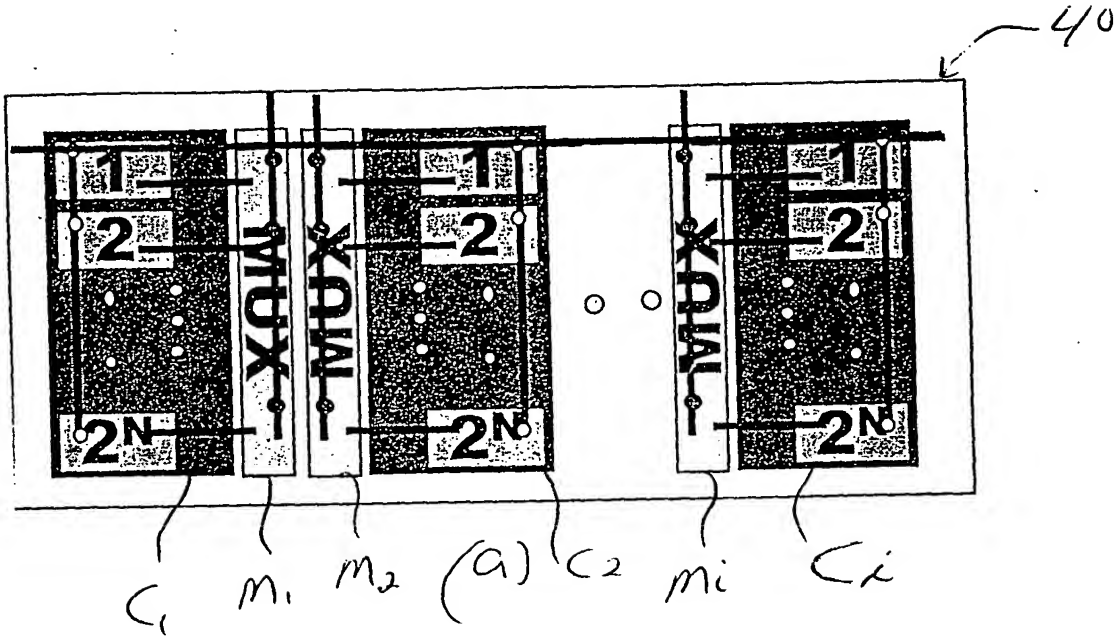

N1
P1
P2
N2
VDD
VDD
VDD
BLC
GND
GND
BLT
VB1
VIN
S1
S2
VDD
GND
N3
VOUT
N4
S4

Fig. 14


40
1
2
2N
MUX
C_1
m_1
m_2
(a)
C_2
m_i
C_i

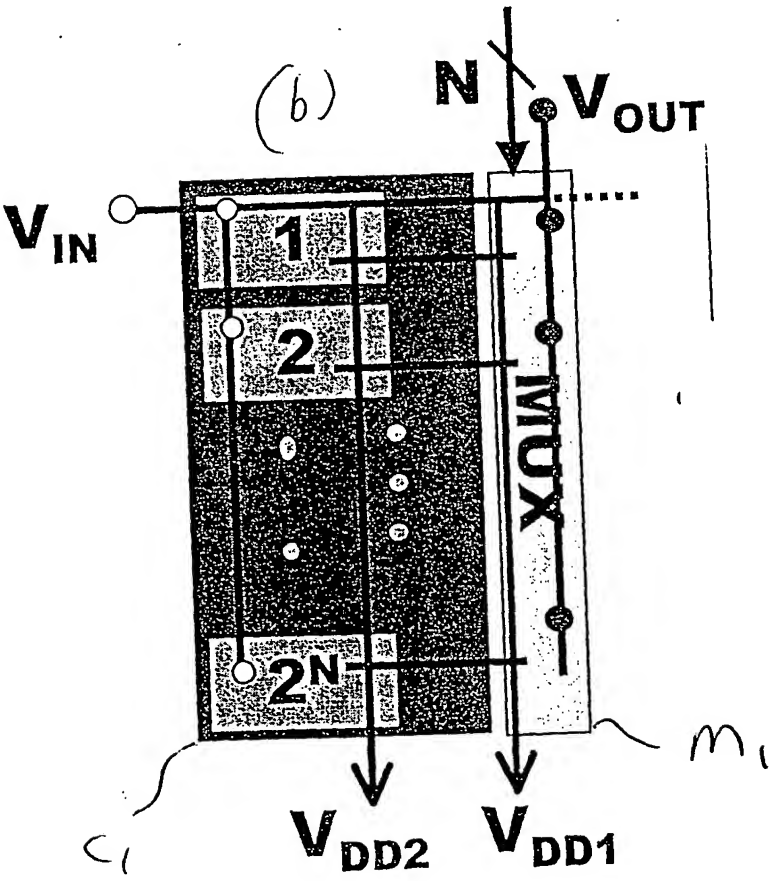

(b)
N
V_{OUT}
V_{IN}
1
2
2N
MUX
m_1
C_1
V_{DD2}
V_{DD1}

Fig 15